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[Joining The RISC-V Ranks: IBM's Power ISA To Become Free](#)



RED2018-102384-T



J. Alastruey, A. Alcolea\*, J.L. Briz, M. A. Dávila\*, C. Escuin\*, R. Gran, P. Ibáñez, A. Navarro\*, L. Ramos, J. Resano, J. Segarra, D. Suárez, E. Torres, A. Valero, M. Villarroya, and **V. Viñals\***  
 \* PhD students contact: victor@vmlizar.es



**Mission** **Vision**

*Research and train researchers in heterogeneous systems and CMPs and their memory hierarchies, focusing on general purpose computing, hard real-time or important applications such as DNA sequencing, Machine Learning or on-board satellite processing*

*Contribute to the design of low-power, high-performance, and reliable processors and accelerators in a open hardware environment, considering different markets, such as intelligent IoT sensors, supercomputers, mobile devices and data center servers*

**Group Profile** **Recent / Ongoing Results**

<b>Research</b>	<ul style="list-style-type: none"> <li>On-chip Multicore Cache Hierarchy: prefetching, replacement, STTRAM</li> <li>Heterogeneous Systems (cpu+gpu+fpga): load-balancing runtimes, accelerators</li> <li>Real-Time systems: static estimation of WCET, temperature-aware scheduling</li> <li>Reliable Systems: permanent, transient, and aging-induced fault tolerance</li> <li>Application Acceleration</li> <li>Embedded Systems &amp; IoT</li> </ul>	<ul style="list-style-type: none"> <li>Architecture and Programming of High-Performance, Low-Power Scalable Computers (TIN2016-76635-C2-1-R)               <ul style="list-style-type: none"> <li>Joint Project with Universidad de Cantabria (2017-20)</li> <li>New Project under evaluation</li> </ul> </li> <li>Gobierno de Aragón reference research group: T58_17R</li> <li>TRAFAIR (2017-EU-IA-0167), Understanding Traffic Flow to Improve Air quality, Connecting Europe Facility (CEF)</li> </ul>	
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<b>Training/Teaching</b>	<ul style="list-style-type: none"> <li>Digital Design</li> <li>Computer architecture &amp; organization</li> <li>Operating Systems &amp; Virtualization</li> <li>Networks &amp; System administration</li> <li>Heterogeneous Systems</li> <li>RT Embedded Systems &amp; IoT</li> <li>Data Centers</li> </ul>	<ul style="list-style-type: none"> <li>Computer, Telecommunication, and Industrial Engineering undergraduate and graduate programs (including Degree and Master Final Projects)</li> <li>PhD program with mention towards excellence</li> <li>Several educational papers on how to teach energy and power in computers</li> <li>Collaborations with other teaching areas: building bridges across the abstraction levels of a computer system:               <ul style="list-style-type: none"> <li>Exposing Abstraction-Level Interactions with a Parallel Ray Tracer. Workshop on Computer Architecture Education, 2019</li> </ul> </li> </ul>
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<b>Innovation</b>	<ul style="list-style-type: none"> <li>Application optimization</li> <li>Accelerator design</li> <li>Citizen science, dissemination of embedded systems &amp; IoT</li> </ul>	<ul style="list-style-type: none"> <li>FCT-18-13586 - Make It Special embedded systems to assist people with disabilities</li> <li>FPGA accelerators for Machine Learning improve the accuracy of the forecast system of Puertos del Estado</li> <li>Accelerating DNA sequencing for intel KNL processors</li> <li>Sending IoT into the atmosphere</li> <li>High-Performance, Low-Power Computer Vision for Virtual Reality (with Eonite Inc. Palo Alto, CA, USA)</li> </ul>	
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**Group positioning & Perspectives in front of Open-Hw & RISC-V**

<b>Re-D++T</b>	<ul style="list-style-type: none"> <li>The RISC-V open Hw/Sw               <ul style="list-style-type: none"> <li>Enables collaboration and can foster our regional markets</li> <li>Is a clear educational path for Computer Architecture and Operating Systems in the undergraduate and master studies</li> </ul> </li> <li>IA accelerators and virtualization for RISC-V cores and related application developments</li> <li>Low power RISC-V cores for IoT with non-volatile cache memories</li> <li>Use RISC-V as innovator driver-thread for universities and collaborative training strategies for all education levels</li> </ul>
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<b>Global Remarks</b>	<p><i>"If many organizations design processors using the same ISA, the greater competition may drive even quicker innovation. The goal is to provide processors for chips that cost from a few cents to \$100."</i></p> <p><i>J. Hennessy &amp; D. Patterson – "A New Golden Age for Computer Architecture" CACM Feb. 2019</i></p>	
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SPARC (Scalable Processor Architecture) is een RISC-processorarchitectuur ontworpen ... Shop now and get Free Value Shipping on most orders over \$49 to the ... and the Fujitsu SPARC64 machines based on the SPARC64-V, SPARC64-VI, ... which individually, are much "weaker" cores than x86 or POWER/PowerPC.. RISC-V is an open-source hardware instruction set architecture (ISA) based on established ... Commercial users require an ISA to be stable before they can utilize it in a product that might last ... Many RISC-V computers might implement the compact extension to reduce power ... "RISC-V The Free and Open Instruction Set".. There could be various reasons why outright processing performance is critical for an application. 4 GHz for Intel ... Will the RISC-V ISA replace X86 and ARM?

An IBM engineer has released the first soft-core implementation of an ... Earlier this month, IBM announced it will follow in the footsteps of the RISC-V gang and open ... the required sections of the Power ISA Specification, will be available ... Join our daily or weekly newsletters, subscribe to a specific section ...

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Incidentally, I think the first consumer devices to adopt RISC-V will be home wireless ... Packard Enterprise, IBM, Microsemi, Oracle, Microsoft, Nvidia, and Qualcomm. ... and low-power real-world implementations in mind. risc-v ... RISC-V is a free to use, modern and open ISA under the governance of .... <https://www.nextplatform.com/2019/08/20/big-blue-open-sources-power-chip-...> [.com/2019/08/23/joining-the-risc-v-ranks-ibms-power-isa-to-become-free/](https://www.nextplatform.com/2019/08/23/joining-the-risc-v-ranks-ibms-power-isa-to-become-free/) .... Compiler Design Tutorial pdf, Compiler Design Online free Tutorial with ... custom, and analog/mixed-signal designs with the best power, performance, area, and yield. ... It can be installed locally with your app with only the packages you need. ... New to RISC-V? Learn Keywords machine learning compiler · self-tuning .... The ATmega16 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced ... If you get to know ATmega16, you can then work with all mega AVRs. ... Atmega16 AVR RISC 8 ... Download freeRTOS & libraries for AVR ATmega for free. ... Join GitHub today. [Salir 'de videos' por la Red](#)



gaZ: group of Computer Architecture  
University of Zaragoza

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